PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 17/50, G06G 7/06 — A1

(11) International Publication Number: WO 95/32478

(43) International Publication Date: 30 November 1995 (30.11.95)

(21) International Application Number: PCT/US95/06527

(22) International Filing Date: 22 May 1995 (22.05.95)

(30) Priority Data:

08/248,311	24 May 1994 (24.05.94)	US
08/316,400	30 September 1994 (30.09.94)	US
08/316,432	30 September 1994 (30.09.94)	US

(81) Designated States: AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TT, UA, UG, US, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, MW, SD, SZ, UG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(71) Applicant *(for all designated States except US)*: IMP, INC. [US/US]; 2830 N. First Street, San Jose, CA 95134 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: KLEIN, Hans, W. [DE/US]; 206 Murcia Court, Danville, CA 94506 (US).

(74) Agents: PARSONS, Gerald, P. et al.; Majestic, Parsons, Siebert & Hsue, Suite 1450, Four Embarcadero Center, San Francisco, CA 94111-4121 (US).

(54) Title: INTEGRATED CIRCUIT HAVING PROGRAMMABLE ANALOG FUNCTIONS AND COMPUTER AIDED TECHNIQUES FOR PROGRAMMING THE CIRCUIT

(57) Abstract

An arrangement of analog circuit modules (21, 23, 25, 27, 33, 37, 39) assembled on a single integrated circuit chip (922) with the ability of the user to program, by serially providing configuration data (Fig. 6) to the chip through its pins (65, 67, 69), certain functions and operational parameters of the individual modules, and to interconnect the modules in a specified way in order to form a desired analog system on the single chip. Software (Fig. 10) running on an ordinary desktop computer system (Fig. 8) assists a user, even though not a highly skilled analog circuit designer, to generate the configuration data, and thus assemble an operational analog system on the circuit chip. The software (Fig. 10) initially displays the circuit modules and other ressources on the chip, without connection between them (Fig. 9), and then builds a picture of the system configuration being implemented (Fig. 16A) as the user selects among operable options listed by the sofware for various module functions, operating parameters and interconnections. When the desired circuit has been formed on the display, the configuration data to implement the circuit is compiled for loading onto the circuit chip. The software also has the ability to display a schematic diagram (Fig. 16B) of a circuit formed on such a chip from only the configuration data stored thereon.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

INTEGRATED CIRCUIT HAVING PROGRAMMABLE ANALOG FUNCTIONS AND COMPUTER AIDED TECHNIQUES FOR PROGRAMMING THE CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates generally to integrated circuit chip products whose internal functions and interconnections are programmable, and, more specifically, to techniques for programming such chip products.

A widely used type of digital integrated circuit contains a large number of basic digital circuit modules which are configurable by a user. A digital system is formed by application of configuration signals to the circuit product. The circuit modules include standard digital circuit building blocks, such as AND-gates, OR-gates, inverters, flip-flops, and the like. Inputs and outputs of these basic digital building blocks are connectable together by switches and interconnecting lines that are formed as part of the circuit. This type of product is commercially known as a field programmable gate array (FPGA).

In one form, the configuration switches are semiconductor pass gates whose states are controlled by the contents of registers that are also provided on the chip, the registers being loaded with the configuration data each time the system in which the chip is a part is powered up or reset. This configuration data is developed, and can be reconfigured, by the end user.

Another popular technology that is not reconfigurable uses anti-fuses as part of the integrated circuit. These connection devices are selectively blown by application of signals to the circuit by the end user

to interconnect the digital modules in a desired manner. The anti-fuses are used in place of the pass gates mentioned in the previous paragraph.

Such configurable digital circuits allow the end user to implement a custom digital system design without having to have a dedicated integrated circuit or gate array designed and manufactured for a single purpose. This permits systems to be built where the volume of production is insufficient to justify the considerable cost of a special single purpose integrated circuit or gate array. Further, in the case of those types of circuits which are reconfigurable, the end user can test a digital system design and alter interconnections between digital logic blocks, as required, before the specific interconnects to be used in the system are finalized.

The extension of this technique to the inclusion of analog circuit modules with configurable digital logic has been contemplated. Such analog circuit modules include amplifiers, comparators, oscillators, voltage and current reference sources, and the like, which can both be configured to some extent and interconnected by the end user from outside the circuit chip to implement a specific analog circuit.

However, the design of such a system of interconnectable analog modules involves different considerations than in the design of the digital logic systems. In the digital domain, the most complex circuits are formed of only a few types of primitives and the communication of binary signals between such primitives makes it relatively easy to group them in modules that can be interconnected together in an almost limitless number of ways to build a complete digital system. Because of limitations in analog circuits and signals which are not

present in the digital domain, such flexibility has not heretofore been provided in the analog domain.

Therefore, it is a principal object of the present invention to provide an integrated circuit including analog modules that approaches the convenience and flexibility of existing FPGAs.

It is also an object of the present invention to provide an arrangement of analog modules, on an integrated circuit chip, that is easily and conveniently configurable by an end user.

It is a further object of the present invention to provide software implemented on an ordinary computer that is easily useable to configure, monitor and test a particular configuration of such an analog signal chip.

SUMMARY OF THE INVENTION

Briefly and generally, a combination of an improved integrated circuit chip architecture and software usable on an ordinary computer makes it easy for a user who is not a skilled analog circuit designer to program the chip for a particular desired end use. A plurality of analog circuit modules are provided with certain specific configurable choices, each of the possible choices resulting in the module operating in a stable and predictable way. An example is a module that is configurable to perform the function of either a buffer amplifier or a comparator, with or without hysteresis, with several operating parameter choices being provided for each function, such as amplifier gain in the case of an amplifier function and a reference voltage or current in the case of a comparator function. By separately choosing each of these functions and parameters in turn, the user is able to program the module into a desired one

of a large number of specific analog signal systems, each of which is operable. The modules are also constructed with input and output characteristics that allow them to be freely connectable with each other in various arrangements through a programmable interconnection network.

Software executed on a personal computer, or a similar system, initially displays on its monitor the symbols (icons) for each of the modules and other resources of the chip in a schematic like manner. As the user clicks on each displayed module in turn, the functional, operational and interconnection choices available for that module are displayed. The user selects one of the displayed possibilities for each category. These selections are immediately displayed, thereby to build in real time a schematic diagram of the system being configured. As soon as the configuration is completed, the final system schematic diagram is displayed with any unused modules or other originally displayed resources being removed from the display. Each choice, or combination of a few choices, causes the bit(s) of one field of a configuration data file within the computer memory to be designated. Once all the choices are made, the completed configuration file is used to configure an actual circuit chip. This is done by loading the completed configuration file into on-chip volatile or non-volatile memory, using it to permanently set fuses or anti-fuses, or to implement any other programmable technology as may be used on the chip.

According to another aspect of the present invention, the configuration software is also adapted to operate in the reverse; namely, to respond to configuration data read from a configured chip product

and display a schematic diagram of the circuit that has been implemented on the chip. This allows the designer to analyze and debug the circuit design. The circuit can be changed by editing the configuration data. Resulting changes in the circuit can be observed on the display which is being updated simultaneously with the configuration data being edited.

The various aspects of the present invention, individually and in combination, provide an integrated circuit chip which processes analog signals in a way that may be easily and rapidly configured, programmed and analyzed by the user. The user can select from a wide variety of individual module circuit options without creating any undesired side effects from the selection of any one option. The user can also interconnect the modules in any of a large number of permitted combinations without affecting operation of the modules or causing harm to the circuit chip. It is preferred to physically limit the individual module programming options and the interconnect possibilities to only those which form stable operating circuit modules and systems. It has been found preferable to do this, rather than allow potentially inoperable configurations which the user, and/or the programming software tool, must know to avoid. The chip product can thus be used by persons who do not possess analog circuit design skills. The programming software tool provided as part of the present invention is thus also simplified.

The foregoing outlines only the highlights of some of the principal features of the present invention. Other features, objects and advantages of various aspects of the present invention are contained in the following detailed description of its preferred embodiments, which

description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a system diagram of a general integrated circuit chip architecture with which the various aspects of the present invention may be utilized;

Figure 2 is a more specific representation of one form of the circuit chip that is generally illustrated in Figure 1;

Figure 3 is an even more specific representation of one form of the circuit chips illustrated in Figures 1 and 2;

Figure 4 shows a circuit included on the chip of Figure 3 to configure analog circuits on the chip;

Figure 5 is a circuit diagram of one representative block of Figure 4;

Figure 6 shows an example configuration data file that is loaded onto the circuit chip of Figures 3-5;

Figure 7 illustrates a format of a command and configuration data when loaded into the system of the circuit chip of Figures 3-5;

Figure 8 generally illustrates a computer system which may be used to generate the configuration data file of Figure 6;

Figure 9 is an example display of the monitor of the computer system of Figure 8 of the resources available on the circuit chip of Figures 3-5;

Figure 10 is a flow diagram which illustrates the processing which occurs on the computer system of Figure 8 to generate the configuration data file of Figure 6;

Figures 11A, 11B and 11C show sequential views of a portion of the display of the monitor of the computer system of Figure 8 with respect to one analog module on the circuit chip of Figures 3-5;

Figure 12 shows example symbols which are displayed to reflect some of the choices made of module functions and operating parameters;

Figure 13 illustrates operation of the computer system of Figure 8 to designate a portion of the configuration data file of Figure 6 which relates to the module to which the views of Figures 11A, 11B and 11C pertain;

Figures 14 and 15 each shows a portion of the display of the monitor of the computer system of Figure 8 when two other of the modules of the circuit chip of Figures 3-5 are being configured; and

Figures 16A and 16B show different versions of a complete monitor display of a circuit that has been configured.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following discussion first includes a description of the circuit chip itself, with respect to Figures 1-7, followed by a description of the computer software used to configure such a circuit chip, with respect to Figures 8-14.

Configurable Analog Circuit Chip Structure

With reference to Figure 1, a programmable analog system is provided on a single integrated circuit chip having one or more signal inputs 801, one or more signal outputs 803 and configuration data input 805 pins, among others. Analog signal input modules 807-809 and

analog signal output modules 811-813 allow for connection of the input and output pins, respectively, to a configurable interconnection network 815. The input modules 807-809 can also include programmable circuit functions, such as buffering, filtering, switching, and other signal conversion functions that enable the chip to be adapted for use in a wide variety of types of analog systems. Similarly, the output modules 811-813 can provide programmable buffers, switching circuits, comparators, and the like. If the circuit chip is designed to interface directly with a digital system, an input module can include a digital-to-analog converter, and an output module can include an analog-to-digital converter. For many applications, there is no need for any other digital processing of the signals being processed by the chip, all the signals otherwise being in analog form. However, such digital signal processing can be included where useful.

A plurality of functional analog circuit modules 817-819 are connected to each other, and to the input modules 807-809 and output modules 811-813 through the configurable interconnection network 815. A wide variety of analog circuit functions can be included in individual ones of the functional modules 817-819, such as amplifiers, comparators, adder/subtractors, filters, rectifiers, and other normally used analog circuits. An individual functional module preferably includes a more complex circuit that is programmable by the user to perform a selected one of two or more such functions. Operating parameters for each selectable function are also programmable, such as the gain of an amplifier, the bandpass characteristics of a filter, the threshold characteristics of a comparator, the level of hysteresis

of a comparator, and similar known analog circuit parameters.

It is also desirable to provide one or more support modules 821 not directly connectable in the analog signal path but which provide support to other modules or configuration circuitry. One example is a bias voltage or current generator whose voltage, current or other characteristic of its output is programmable. Another is a clock oscillator having programmable frequency clock signals. A programmable auxiliary circuit 823 is also desirable. A test module 825 allows connection of a pin 827 to a selected node within the chip, such as a signal node within interconnection network 815. Programmable power control circuits 829 are also desirable in order to specify which modules are to operate in a reduced power state during periods of non-use.

In order to program all the modules in the system and interconnect the input, functional and output modules together to form a customized operable analog circuit between the input and output pins, a digital configuration circuit 831 is provided. Data loaded through pin(s) 805, in serial or parallel form, is used to make connections within each of the other blocks shown in Figure 1. In a preferred form described in more detail with respect to Figures 2-7, the configuration circuit 831 includes a plurality of series connected registers which are loaded with configuration data through the configuration data input pin(s) 805. Those registers are of a volatile type but could be formed on non-volatile memory if desired. Specific fields of the configuration data registers are connected to program operation of individual modules and to interconnect them through the network 815. A capability is also provided to dynamically

change the contents of individual ones of the registers during operation of the circuit, thus allowing a host system in which the circuit chip is used to reconfigure at least one function, connection or operating parameter of one or more modules, an ability that is not available with usual analog circuits. Configuration data to be loaded into these registers upon initialization of the circuit chip may be stored in non-volatile memory provided on the chip in a manner that any dynamic changes made during operation do not affect the contents of the memory.

The interconnection network 815 may be implemented in a number of ways. It can be a full cross-bar type of network, for example, in order to allow a maximum flexibility of the interconnections which are possible. However, since only a limited number of connections need be provided, as will become more apparent from later descriptions herein, the overhead associated with such a network is not justified. Therefore, a more limited type of interconnection network 815 is utilized. This may be one of the many types used in or proposed for field programmable gate arrays (FPGAs) but those networks are also usually more complex than necessary. The specific devices used within the network 815 to make selected interconnections between conductors can also be selected from a wide variety of known types, such as fuses, anti-fuses or volatile pass transistor switching networks. The later type of switching device is preferred herein since this allows easy reconfiguration, including the making of changes in the circuit as part of its operation.

A preferred interconnection network 815 is illustrated in the somewhat more specific system of Figure 2. The module interconnection network 815 includes a bus

having a number of signal paths (signal highway) with one or both of the internal input or output of the individual modules being connectable to one or more of the internal bus signal paths. In this example, the bus is shown in two portions 833 and 835, joined by a switching network 837. The switching network 837 can be designed to connect various ones of the conductors of the bus portion 833 to those of the bus portion 835, or simply be able to break certain of the bus conductors into two isolated segments. Any such connections can be placed under the control of the configuration circuits 831, and are useful when a larger number of modules is utilized. It is not employed in the specific embodiment described with respect to Figures 3-7, wherein a single bus segment exists.

The connection of the modules to specific conductors of the bus segments 833 and 835 is shown in Figure 2 with a high degree of generality. The input modules 807-809 have their individual outputs connected to a selected one or more of the bus conductors through switching circuits 839-841, in response to respective control signals from the configuration circuits 831. Similarly, the output modules 811-813 have their individual inputs so connected through switching circuits 843-845. The functional modules 817-819 have inputs connected to one or more bus signal paths by switching circuits 847-849, and outputs by switching circuits 851-853. A switching circuit 855 connects one or more of the conductors of the bus to the test module 825, for outputting through pin(s) 827.

Such a high degree of flexibility in controlled connections of the modules to the bus is usually not necessary, however. However, either all the module inputs or outputs may be permanently connected to a unique bus

conductor. The other of the internal input or output of the individual modules is then selectively connected to a designated number or all of the bus signal paths by switching circuits, in response to control signals from the configuration circuits 831. This more limited interconnectability is implemented in the embodiment of Figures 3-7 described below.

The functional modules 817-819, and to some extent the input modules 807-809 and output modules 811-813, may be made to operate with either voltage or current analog signals. The best type of circuit technique to be employed within the modules depends upon the frequency range, bandwidth, amplitude, noise tolerance and other characteristics of signals with which the circuit chip is expected to be used. In either case, the internal input and output interfaces of the interconnectable modules are constructed so that their operation and effect on the analog signals are substantially independent of which other modules are interconnected together and any variations of impedance or other characteristics between specific module interconnections. The modules are constructed to be interconnected together in a wide variety of different combinations according to the desired overall circuit intended to be configured, all without the quality of the analog signal or operation of the individual modules being adversely affected by any of a large number of different possible connection paths being utilized between the input, functional and output modules.

In the case where the signals are carried within the individual modules by a varying voltage (voltage mode) and communicate voltage varying signals between modules, the input impedance of each such module is made to be very high, and the output impedance is made to be very low. In

the case where the modules carry signals as current variations (current mode) and communicate current varying signals between modules, the input impedance of each such module is made to be very low and its output impedance made to be very high.

The specific circuit chip embodiment of Figures 3-7 will now be described. Several pins of the circuit chip are designated for receiving input signals, a single line 11 and a group of lines 13 being shown connected to such pins. (Figure 3) Similarly, several of the circuit pins are designated for carrying output signals, lines 15, 17 and 19 being individually connected to such pins. The input signals are applied to a circuit configured from a plurality of functional analog circuit modules, three such modules 21, 23 and 25 being illustrated in this example. Generally, many more such functional modules may be included on a single integrated circuit chip.

Each functional module contains an operating circuit. The analog circuits implemented by individual functional modules include one or more amplifiers, one or more comparators, filters, and the like, at least some characteristics of which are programmable by the user. This is preferable to providing a mere assembly of transistors which must be programmably interconnected in order to form any operable circuit. The characteristics of the circuits which are programmable by the user include the gain of an amplifier, the threshold characteristics of a comparator, the bandpass characteristics of a filter, and the like. An individual functional module usually includes one such circuit but can alternatively have two or more such circuits. Also, one or more modules may be included that contain only passive components, such as a programmable resistor or capacitor circuit. The

particular functions that are provided in the plurality of functional analog circuit modules included on any particular integrated circuit chip will, of course, be selected to be those useful for the range of applications for which the circuit chip is being provided. In this example, the functional modules 21 and 23 are programmable amplifiers and the module 25 is an adder/subtractor circuit.

In addition to the plurality of functional modules processing the signals between the input and output pins if the circuit chip, circuit modules are also included at the input and output of the circuit. For example, an input circuit module 27 receives a signal in the line 11 and outputs it in a line 13. The input module 27, in this embodiment, includes a filter having leads 29 and 31 connected pins of the circuit. This allows an external capacitor to optionally be connected as part of the filter. The filter is connected to a programmable amplifier, whose output is connected to the line 12.

One of several input lines 13 is, after some processing, effectively connected to an output line 35 by an input module 33. The input module 33 includes a multiplexer 124 which selects one of the input lines 13 for connection to an input of a filter 125. The multiplexer 124 may be operated either directly by configuration bits (Figure 4), or may be designated by a different set of configuration bits to allow the multiplexer to be switched in response to an external signal applied to two pins connected to lines 861. An output of the filter 125 is applied to one input of a programmable amplifier 631, whose output is in the line 35. A programmable offset voltage source 633 is applied to a second input of the summing amplifier 631. A

programmable bias generator 113 could alternatively be used to generate the offset voltage.

Similarly, output modules are provided, two such output modules 37 and 39 being shown in the example system of Figure 1. Typically included in an output module is a buffer amplifier but other circuit functions may also be included, such as a filter, comparator and the like. In this example, the output module 37 includes a programmable comparator 865 having one signal input 867 and a programmable reference voltage source 863 connected to a second input. This allows a selection of the function of the module between a buffer amplifier, wherein the reference voltage source 863 is not used, and a comparator, wherein the reference is used. A second output module 39 contains two such circuits which may be operated independently or together to provide a window comparator as another function. Each of two comparators 134 and 135 has one signal input 136 and 137, respectively, and a programmable voltage reference 139 and 140. When operated as a comparator, either of the output modules is effectively an analog-to-digital converter, providing a digital output.

Each of the input, functional and output signal modules described above are interconnected over a bus 41 (signal highway). Each signal path of this example bus 41 is a single electrical conductor, or pair of conductors, depending upon the type of analog signal that is being communicated over the bus. In the architecture of the Figure 3-7 example, the outputs 13 and 35 of the input modules, and outputs 22, 24 and 26 of functional modules, are permanently connected with a unique one of the signal paths of the bus 41. The inputs to the functional and output modules are selectively connected to individual

signal paths of the bus 41. That is, the specific bus signal paths to which the module inputs are connected are programmable by the user. This arrangement is advantageous when the modules operate in a voltage mode, since the module outputs can simultaneously drive more than one other module. However, this is preferably reversed for a chip where the modules operate in a current mode; namely, the inputs of the functional and output modules are permanently connected with unique ones of the bus signal paths, and the outputs of the input and functional modules are selectively connected to various of the signal paths. This is because the inputs of current mode modules can accept more than one current output of other modules.

All of the signal modules described above are configurable in one or more of the following ways: (1) the function performed, (2) operational parameters when performing that function, (3) the circuit of the bus 41 to which connection is made. Other configurable modules may be used which are not in the signal path between input lines 11 and 13, and output lines 15, 17 and 19. One such module is a test probe module 110 which includes a buffer amplifier 130 having an input line 131 that is connectable to any of all, or nearly all, of the signal paths within the bus 41. This allows an output 112 of the amplifier to be connected to any one of the signal paths of the bus 41. The user of the integrated circuit chip then has direct access for test purposes to signals on the bus 41 internal of the chip. Provisions can also be made to selectively connect the input of the amplifier 113 to other analog signal nodes within the chip. The test probe module may also include one or more amplifiers, optional filters, and the like, in a signal path from a selected bus circuit to

the output 112, any of which can be made to be programmable. Further, provisions can be made to bring internal digital signals to the test module output 112. An example of such a digital signal is a serial stream in a line 722 of the configuration data stored on the chip. This then allows the user to read out the configuration data for trouble shooting and the like.

It is also sometimes desirable and useful to provide a reference voltage output in a line 116, so a module 117 may be provided for this. The reference voltage is set by properly configuring the module 117. Similarly, it is sometimes desirable to include an analog signal module 119 that has both inputs 120 and an output 121 connected to external pins. This circuit includes a programmable gain amplifier 147.

The clock oscillator 75 is optionally made to be configurable. Such configuration can include the setting of frequency dividers in order to set the output frequency or frequencies of the clock circuits 75. A power control circuit 865 is also configurable to set a characteristic of a power down system.

The configuration circuits of the example chip of Figure 3 are separately shown in Figure 4. Each of the modules of Figure 3 includes a configuration circuit. A configuration circuit 43 (Figure 4) is part of the input module 33, a circuit 45 within the functional module 25, a circuit 47 within the functional module 23, a configuration circuit 48 within the input module 27, a circuit 49 within the functional module 21, a circuit 51 within the output module 37, and configuration circuits 53 and 54 within the output module 39. Similarly, the test circuit 110 contains a configuration circuit 111, the auxiliary circuit module 147 a circuit 123, the external

reference module 117 a configuration circuit 118, the bias generator 113 a circuit 114, the clock module 75 a configuration circuit 72, and the power control module 865 a circuit 48.

Each of the individual module configuration circuits includes a shift register. These shift registers are connected in series to receive configuration data over circuits 55. That is, binary data is serially shifted along this series connected number of shift registers to reach desired configuration circuits within one or more of the modules. The serial input circuit 55 through which such a binary signal is introduced includes one line for the binary signal, a clock line for providing clock signals to each of the shift registers in order to move the data through them in sequence, and potentially other control lines. These lines are extended between the output of one shift register to an input of another shift register, such as by a segment of lines 57 extending between the configuration circuits 43 and 45, a segment 59 between the configuration circuits 45 and 47, and so forth. In addition, each of these configuration circuits receives additional control signals over lines 61. Signals in the lines 55 and 61 are generated by a configuration control circuit 63.

A user of the integrated circuit chip of Figures 3-7 serially loads this binary configuration data through a pin of the circuit's package onto a line 65, along with an accompanying input clock signal in another line 67 from a separate pin. A load control signal applied to yet another pin provides a signal in the line 69 which operates to both select the chip for receiving configuration data and to latch that data into each of the modules' configuration circuits after receipt. A load

control output signal in a line 71 is generated for use when several chips are connected together in a daisy chain arrangement.

A non-volatile memory 73 (Figure 4) is provided as part of the integrated circuit chip in order to store the configuration data desired by the user to be initialized in all of the modules' configuration circuits. The preferred type of memory is an EEPROM. This data is loaded by the user through the line 65 along with the user's clock signal in line 67, and then by way of circuits 74. Since the configuration circuits within each of the modules includes volatile memory, the configuration data is written into the modules from the memory 73 upon the circuit chip being powered up. This internal operation is synchronized to an internally generated clock signal in a line 76 from a clock oscillator 75. The configuration data stored in the memory 73 is shifted with the internal clock signal in line 76 into the series circuit of configuration shift registers through circuits 55. Because of the rewriting capability of an EEPROM, the memory 73 may be reloaded periodically by the user, as desired.

The configuration data stored in the memory 73 can remain in the configuration circuits of the modules without change during operation of the circuit but the configuration capabilities of this circuit also allows the user the periodically change the configuration of all the modules or a selected one or more of them at a time, during operation of the system. This new configuration data is applied through the input lines 65, 67 and 69 from their respective pins.

The format of externally applied configuration data is shown in Figure 7. A first byte 85 which precedes

such data is decoded within the control circuits 63 in order to determine what is to be done with the data. A next byte 103 specifies the number of bytes contained in the data 104 which immediately follows. The command byte 85 can, for example, specify that this data is to go into the memory 73 or directly into one or more of the serially connected registers of the configuration circuits shown in Figure 4. The command byte 85 can also be used for purposes other than introducing data into the circuit chip. A command decoder as part of the control circuits 63 decodes a command from the data block 85, which can be used to execute any operation on the chip that is designed to respond to a specific command byte.

An example of the structure of each of these configuration circuits is shown in Figure 5. Typically, the configuration circuit 43 includes a shift register 98 that is either included within the series connection of shift registers or bypassed, depending upon the setting of semiconductor switches 99 and 100. These switches are set by the select signal in the control circuits 61. If the configuration circuits 43 are addressed by the command byte 85 (Figure 7) of the data being received in the line 65, then the switches 99 and 100 are actuated to connect the shift register 98 in the series circuit. Otherwise, the switches 99 and 100 cause the configuration data being loaded to bypass the shift register by substituting a conductive path 101. Once the shift register 98 has received data, it is transferred to a configuration register 105 in response to a load signal within the control lines 61. This transfer occurs simultaneously in each module. The contents of the configuration register 105 are decoded by a decoder 106 to provide the switch controlling signals in the lines 107. This arrangement

allows new configuration data to be introduced into the shift registers of addressed modules without affecting operation of the modules. Issuance of the load signal then instantly transfers the new data in parallel into the configuration registers of the addressed modules in order to change their configuration.

Although semiconductor switches are schematically shown in Figure 5 as a convenience in explaining the operation of the circuit, logic gates, such as two or more NAND gates, connected in the form of a multiplexer (MPX) are usually employed to perform the switching function. The term "shift register" as used in this description is intended to refer to each group of storage cells, in the long series connected circuit formed of such cells, which can be bypassed by a single switching circuit of the type just described. The serially connected shift registers in each of the modules can have different capacity depending upon the number of choices provided for operation of the modules controlled by the data stored in the register.

The ability to address less than all of the 14 serially connected shift registers in the configuration circuits of Figure 4 allows rapid rewriting of a selected one or a few of them without having to reload the entire chip. This is a significant advantage. The contents of one or more shift registers can be dynamically changed as the circuit chip is operating. This can be done by a host system in which the circuit chip is a part, or by a user during programming and debugging of the chip configuration. The advantages of serial loading of configuration data, the need for use of only a few pins among them, are combined with the advantages of random access of portions of the configuration data file. It is

preferred that such dynamic configuration not affect the contents of the memory.

Referring to Figure 6, an example of the contents of the module configuration registers of Figure 4 is given. These contents are illustrated in the form of a bit stream that is one bit wide, representing that which is loaded into the registers of Figure 4 from the control circuits 63 during initialization of the circuit chip described with respect of Figures 3-5. In the example of Figure 6, one group 869 of contiguous bits is positioned in the bit stream so that it is loaded into the configuration register 43 (Figure 4) of the input module 33 (Figure 3). A next contiguous group of bits 871 is loaded into the configuration register 45 of the functional module 25. A group 873 of bits, appearing later in the bit stream, becomes loaded into the configuration register 48 of the input module 27, a group 875 in a configuration register 51 of the output module 37, a group 877 into the configuration register 123 of the auxiliary module 119, and a group 879 loaded into the configuration register 72 within the clock oscillator module 75. Similar groups of bits exist for each of the other configuration registers shown in Figure 4 but are omitted from Figure 6 for simplicity.

Each such group of bits includes several fields. For example, the group 869 (Figure 6) which controls the input module 33 (Figure 3) include a field 881, the bit values of which control the gain of the input amplifier 631. The bits in another field 883 control the power of the input module, designating whether that module is powered down individually when it is not used and/or whether it is powered down upon a global power down command. Another field 885, in this example being only

one bit, designates whether the filter 125 of the input module 33 is to be included in the circuit. Another field 887 controls operation of the multiplexer 124 of the input module 33. The binary contents of this field can either directly control the switching operation of the multiplexer 124, or control whether or not the multiplexer 124 is switched in response to signals from external pins over lines 861, or both. This particular module example, as with the others being described is meant to be exemplary of the types of things that can be controlled by the configuration bits within the one bit stream that are designated for loading into a particular module.

The group of bits 871 (Figure 6) includes a field 889 which controls the gain of the amplifier within the adder/subtractor functional module 25 (Figure 3). A field 891 controls the power saving operation of this module, as is the case with most of the other modules. Another field 893 controls whether one or two inputs are to be used, and their respective polarity. A final field 895 designates which of the conductors within the bus 41 the inputs of the module 25 are to be connected.

A field 897 in the group of bits 873 sets the gain of the amplifier within the input module 27, and another field 899 controls its power down response. Another field 901 designates whether the filter of the input module 27 is to be used or not, and, if so, whether the external connections 29 and 31 are to be provided. These external connections can be used to add a capacitor or other off chip component to the on chip filter of the input module.

For the output module 37 (Figure 3), a field 903 (Figure 6) sets the output voltage of the voltage reference circuit 863. This circuit can be configured to

be, in effect, an analog-to-digital converter. Another field 905 of bits sets the operating mode of the output module. These bits select whether the module operates as a simple buffer amplifier, which then does not utilize the voltage reference source 863, or as a comparator, when that reference source is used. Another field 907 controls the power down response of the module 37, and another field 909 establishes a connection between the input circuit 867 and one of the signal paths within the bus 41.

One optional but very useful variation of the configuration system described with respect to Figures 5-7 expands the size of the shift and configuration registers in one or more of the modules in order to store alternative configuration data. A larger configuration register stores two or more (such as four) different sets of bits for at least selected ones of the function, operating parameter and interconnection fields. A multiplexer is then introduced between the configuration register 105 (Figure 5) and the decoder 106 to select which of the alternative fields contained within the configuration register is to be decoded at any one instant for configuring the module. The multiplexer within a given module is controlled by the user through either the contents loaded into another configuration register field of that same module or a selection signal applied to the multiplexer by connection to external pins. This same multiplexer control signal can be applied to such a multiplexer of two or more modules in order that their function, operating parameters or interconnections are switched together. The input signal multiplexer 124 (Figure 3) can be operated by the same control signal, thereby allowing one or more modules to be automatically

switched into a unique configuration for each of the input signals.

The example circuit chip is preferably designed so that each module operates in a stable and predicable manner, as described above, no matter what bit pattern a user tries to load into the module's configuration registers. This is accomplished with a combination of the specific circuit implementations and computer software provided for generating the configuration bit stream of Figure 6. Such software is described in the next section with respect to Figures 8-15.

In order to be able to read out the configuration data from a programmed circuit chip of the type of Figures 3-7, the line 722 (Figure 3) to the test module 110 is connected as an output of the last configuration circuit 48 (Figure 4). Thus, in order to read out the data in the configuration registers, that data is first loaded into corresponding ones of the shift registers. The serial data stream in the shift registers is then shifted out through line 722 and thence to a pin on the chip. Since the contents of the configuration registers are not changed by this configuration data readout, operation of the circuit is not interrupted during the readout process. The serial configuration bit stream is preferably reintroduced at the same time into the shift registers through the line 55 (Figure 4) by forming a data loop pattern, so the configuration data in the shift registers is restored to that which existed before the data was read out. Alternatively, the configuration data read out of the chip can be altered in some desirable way before being reintroduced to the shift registers. This is accomplished an external computer running the configuration software described in the next

section. The contents of at least any shift register that has been changed are then loaded into corresponding configuration registers for changing operation of the circuit chip.

Configuration Software

The configuration software of the present invention is preferably executed on a general purpose desktop computer, such as schematically illustrated in Figure 8. As is well-known, such a computer includes a monitor 911, entry devices including a keyboard 913, random access memory 915, a central processing unit 917, and disk storage 919, among other units. The bit stream of Figure 6 may be generated for a particular application by such a computer system alone, with the software to be described. However, it is usually preferable to connect an evaluation board 920 to the computer system, wherein such a board includes an integrated circuit chip 922 in accordance with that described with respect to Figures 3-7. This then allows the configured bit stream of Figure 6 to be loaded into an actual chip for testing purposes. The evaluation board is connected to allow such loading and also provides terminals 924 connected to the various analog signal inputs and outputs of the chip. The user can then test a chip with actual analog signals after being loaded with the configuration data developed with the aid of the computer software. The software allows the configuration data to be reconfigured and reloaded, and then retested with actual analog signals, either for one or more individual modules or the entire configuration data bit stream.

When a user first begins to use the configuration software, a schematic display of the

resources of the integrated circuit chip is provided on the computer monitor. A sample display is illustrated in Figure 9 for the specific example of the circuit chip of Figures 3-7. Each of the modules and other available components are illustrated, being given the same reference numbers in Figure 9 as used in Figure 3 but with a prime (') added. It is significant that all of the circuit chip resources are initially displayed so that the user can see at a glance what is available for his or her use.

The only interconnections that are shown on this initial screen display are those which are permanently wired. As the user specifies various programmable interconnections of these modules and other resources, they are also displayed. Alternatively, the available interconnections could also be shown, such as in a different color or a background grey, from which the user can directly select in order to interconnect the various modules. In either case, there is progressive documentation on the screen of the system being configured. In addition to each interconnection being displayed as soon as it is specified by the user, the functional and operational parameters selected by the user are similarly displayed as part of the module icons. When the user has completed the configuration of a system, any unused modules or other resources initially displayed on the screen are removed. What is left is a block diagram of the configured circuit chip. The configuration software is preferably utilized in a Windows or Macintosh environment, or something similar, with pull down menus, the ability to "click" a cursor on a portion of the display to allow operating on that display, and so forth.

Figure 10 is a flowchart of an example operation of the configuration software. A first step 915 calls for

the computer system of Figure 8, when programmed with the configuration software, to recognize when the user has designated one of the modules of the display of Figure 9 to be configured. One module is so configured at a time. The user will designate such a module either by clicking the cursor on it or typing in a unique designation. Once a particular module has been selected, the software displays further choices to the user from which the functional operation of the selected module may be specified (steps 917-923), the selection of various operational parameters for the module (steps 925-931), and the interconnection of the module (steps 933-939). Each of these three designations (function, operational parameters and interconnection) is described herein as being set in separate sequential steps but, alternatively, all three can also be specified in a single selection step.

The configuration process of Figure 10, as executed by the software, will be described with respect to the configuration of one of the output modules. Figure 11A illustrates a display which appears on the computer screen, at the step 919 of Figure 10, since the module being configured at this time does allow the user to select among different functions. Four such functions are shown in the display of Figure 11A, the user being able to select one of them by clicking the cursor on one of the choices. Once such a selection is detected to have been made in a step 921, that selection is displayed, as shown in the top part of the display of Figure 11B. The function of a buffer amplifier is shown to have been selected, in this example. At the step 923, any of the configuration bits within the data stream of Figure 6 which this choice causes to be specified are then

designated for the proper bit positions within the configuration data bit stream of Figure 6.

A next step 925 initiates a second set of options from which the user can choose. These are choices among various operating parameters for the output module when configured to perform the function earlier selected, in this case that of a buffer amplifier. A display of such operational choices appears in the bottom part of that of Figure 11B. As shown in Figure 11B, certain commonly used settings are initially displayed but the user has the ability to scroll to other choices by clicking the cursor on the up-down arrows adjacent each such default display. The software, at a step 929, awaits the user clicking on the "OK" box of the display in Figure 11B to indicate that his or her choices have been completed. The final set of operating parameter selections remain displayed. Any bits of the configuration data for this output module which are set by such choices have thus been designated.

Data tables within the software specify the functions that each module can perform. Other data tables identify the various operational parameters that can be controlled for each such function. These tables are static, not being changed during the process of configuring a circuit. It is from these tables that the displays of Figures 11A and 11B are obtained. The available operating parameters of such tables can be displayed directly or some processing can occur before such a display. For example, in addition to the operating parameter choices for a given module depending upon the function selected, they can depend upon earlier designated configuration parameters. Showing a different resolution of a voltage or current to be set is another example,

either as a result of earlier related configuration choices or as a result of a choice by the user. In the latter case, the first line of the displayed operating parameters is the resolution desired by the user, and the possible incremental change of the parameters shown on the same display is then immediately changed to that so selected.

Since the output module also has an input which needs to be connected to an output of another module, a display of the potential connections is given, such as shown in Figure 11C, at step 935 of the software operation. Another static table used by the software contains this information for each connectable module. That display includes a designation 941 of one of the functional modules whose output is connectable to the input of this particular output module. The various functional modules that are so connectable can be viewed by the user scrolling through a list of them by clicking on the up-down arrows adjacent the display 941. Once the user clicks on the "OK" box of the display of Figure 11C, the software, at step 937, knows that the interconnection selection process has been completed. As noted in a step 939, that interconnection is then added to the display of Figure 9, as shown in Figure 11C. That is, the input of the output amplifier 865' as shown to be connected to the output of the functional amplifier 21'. As each module is configured, one at a time, these interconnections are established and added to the display of Figure 9 so that the user always has an overall view of the circuit that has been configured so far.

An alternate way to display and select interconnections is to show the possibilities provided on the circuit chip in a background grey or contrasting

color. The user clicks on one of the interconnection possibilities, which is then boldly shown on the monitor as a conductive path. Yet another alternative is to provide for a user to click on both ends of a desired conductive path, which is then established on the display.

The example being described is for configuring a circuit chip which is implemented with voltage signal modules, either which operate with in a continuous voltage mode or in a charge mode (switched capacitor circuits). If, on the other hand, a circuit chip having modules operating with signals in the current mode is being configured instead, it is then a module's output which is designated for connection to an input of another module. It should also be remembered that the configuration software example being described is for a circuit chip having a limited interconnection network including the bus 41 of Figure 3 with either the inputs or outputs of the modules permanently connected to individual ones of the bus signal paths. If a more general interconnection network is employed instead, such as described with respect to Figures 1 and 2, the user may be given additional interconnection choices. For example, the user may need to specify the connection of both the input and output of each functional module.

At a step 943 (Figure 10) the software cycles back to the beginning step 915 to implement the same process for another module. This continues until the user indicates that the configuration is complete. At that time, a design rule check is made by the software, as indicated by a step 945. Although, as stressed earlier, the circuit architecture and software tools are designed to make sure that all allowed configuration choices result in each module operating in a stable manner and as

otherwise desired, the user can still make some undesirable and perhaps even inoperable interconnections of the modules. An example is when an incomplete connection exists between the circuit input and output pins. If there is a break in the signal path, the configured circuit will, of course, be inoperable. Another example is when an output of an amplifier is connected to its input, often an unintended configuration. A further example is when power remains connected to a module that has not been connected into the signal path of the circuit. Finally, since the most gain in an analog circuit is desired to exist at the input, in order to minimize the effects of noise, a user would like to know if his or her configuration does not satisfy this condition. Therefore, a check is made at the end of the user's configuration as to whether any such invalid or undesired combinations have been specified, in a step 947. If any are found, the user is given the opportunity, in a step 949, to make a change before the configuration is completed but is not required to do so.

When no invalid or undesirable choices exist, and when the user has been given an opportunity to change any noted undesirable choices, the software, in a step 950, performs any desirable post-processing. One such item of post-processing is accomplished when the internal modules are formed in a charge mode with signals being communicated between them in a return-to-zero (RTZ) or other discrete time format. This requires that two modules which have been connected together be driven by clock signals having a proper relative phase, in order to communicate such signals between them. These modules are provided with means for selecting that phase. This is done automatically by the software, once the user has

designated the module interconnections. As a last step 951, the entire configuration file is assembled into the form illustrated in Figure 6.

In addition to showing the connections between the modules as soon as they are designated, the function and parameters set for each of the modules are similarly immediately displayed. Examples of some symbols which can be used are given in Figure 12. An symbol 963 for an amplifier shows the polarity and amount of gain which has been set. A symbol 964 outside of the amplifier symbol indicates that this module has been included in a group of modules that are selectively powered down in response to a particular power control signal. The absence of this symbol 964 means that the module will so power down only if the entire chip is set to power down. A symbol 965 indicates that a module has been configured into an inverter. A buffer amplifier, with its selective power down feature turned on, is indicated by a symbol 967. That of 969 indicates a comparator, and that of 971 a comparator with hysteresis. The symbol 973 reveals that an amplifier has been set with a larger than normal output driving capability. Of course, any easily recognized symbols can be employed, the important point being that they are presented on the display as soon as the choices which they represent have been made.

A simplified example of how the configuration software builds the configuration data file is given in Figure 13, with respect to the configuration of the output module 37, as previously described with respect to Figures 11A, 11B and 11C. It is a portion 953 of the configuration data file that is being designated by the user making the choices previously described. A data table 955 within the configuration software for this

output module identifies a particular bit combination ("xx") for each of the four functions from which the user has to choose. When one such function is chosen, two such bits of the configuration data file are specified, in this general example. Similarly, a table 957 exists for the operating parameters which are selected by the user from the display of Figure 11B. Each of the choices of the operating parameters also has a certain bit value or bit values, which are then transferred to other bit locations within the configuration data portion 953. Similarly, another table 959 is so used to list the available connections from which the user may choose and, when the choice is made, to insert bit values in the field of the configuration data that effect that choice. Each of the tables 955, 957 and 959 (really part of a single table specifying bit pattern choices for all of the different fields of the configuration data) is unchanged during the configuration. That conversion data table is specific to the type of chip being configured.

An alternative type of screen display is shown in Figure 14 where the user may make all the choices with respect to one module, in this case the adder/subtractor functional module 25, at one time. All of the choices of its function, operating parameters and input terminal connections are provided on this one display. The user can see all of the permitted possibilities for each of the parameter and interconnection choices that are displayed, by clicking on the arrow adjacent each such item. Once the display of the selections is the correct one, the user clicks the "OK" box and the display changes to show the interconnection and the bit pattern for the portion of the configuration data of that module is then generated. A

similar one-step display is shown in Figure 15 for the input module 33.

Figure 16A shows an example of the display of Figure 9 after a specific circuit has been configured. It will be noted that several of the available modules have not been used as part of this exemplary designed circuit. These can be shown muted or in a color that is different from that of the active circuit portions. It is also desirable to be able to show on the computer monitor the diagram of the configured circuit without showing any unused modules or other elements. Figure 16B shows such a version of the display of Figure 16A. The user/designer can designate the form of the display.

If an actual circuit chip is connected to the same computer system, as illustrated in Figure 8, the user also has the option to load that configuration file onto the shift registers of an actual circuit chip through the data input lines 65, 67 and 69 (Figure 4) for testing purposes. Signals are then applied to the configured chip inputs 11 and 13 (Figure 3) while signals at its outputs 15, 17 and 19 are monitored. Various operating commands, other than to load the configuration data into the shift registers, can also be issued from the computer system and loaded through the configuration data inputs 65, 67 and 69. Convenient commands which are provided include one to write the configuration data file to the on-chip non-volatile memory 73. Another command loads the shift registers with the configuration data already stored in the on-chip non-volatile memory. Yet another is to switch the multiplexer 124 (Figure 3) to select one of the signal inputs 13. This switching is accomplished by addressing a particular field of the serial registers which contains the input multiplexer control bits, and then loading a new

bit pattern in that field. When loaded into an accompanying configuration register by a load command, the multiplexer 124 is then switched. Other useful commands set the circuit chip power down characteristics, clear the configuration registers, and initiate a calibration operation which sets an offset voltage applied to a received signal in an input module.

Further, the test probe module 110 (Figure 3) or 825 (Figures 1 or 2) can be operated by the user from the computer system of Figure 8 to connect an internal node of the circuit to an output pin for monitoring analog signals at various selected internal nodes. When the test probe module is so used, the display of the configured circuit is visually highlighted in some manner to indicate the node to which the test module is connected. This highlighting can take the form of displaying an interconnection between modules, or a portion thereof, with a different color, boldness or flashing. The test probe function is initiated by another command entered through the inputs 65, 67 and 69 (Figure 4), followed by data which specifies the signal path of the internal bus 41 (Figure 3) to which the input 131 of the test probe module 110 is to be connected. Other data which specifies operating parameters of the test module 110 can also be included if the amplifier gain or other parameters are made to be configurable.

The test probe module 110 can also include additional circuitry to allow access through the external line 112 to internal digital portions of the circuit chip. The test probe then contains additional circuitry for interfacing with digital signal nodes of the chip. One application of the digital test capability is to read out through the line 112 the contents of the configuration

registers, as previously described. This is again accomplished by an appropriate command, which addresses the shift register in the test module, followed by configuration data for that register. Whether an analog or digital circuit node is being accessed, operating parameters of the test module circuitry can also be controlled by the contents of a configuration register within the test module.

The signal input(s) 11 and/or 13 (Figure 3) will generally be connected to a conventional external signal source, such as a signal generator, during a test of the circuit chip 923 (Figure 8). One or more of the outputs 15, 17 and 19 can then also be connected to a conventional piece of signal analyzing equipment, such as an oscilloscope. Alternatively, the configuration software can include the ability to display these output signals on the monitor 911 (Figure 8), either on the same screen which contains a display of the final configured circuit being tested or on a separate screen. Multiple signal waveforms can be displayed, including one from the output 112 (Figure 3) of the test module.

It can be seen that this configuration software allows the user to fully test a particular configuration of the circuit chip. In addition to the various commands listed above, configuration data in individual configuration registers can be changed by causing the appropriate command to be sent to the chip configuration control 63 (Figure 4) to address an individual register, followed by new data to be loaded in that register. The effects of this change in configuration can then immediately be observed by the user.

If a chip part has already been configured, or if a configuration data file has been generated, it is

often useful to be able to easily ascertain the actual circuit that is, or would be, implemented by the existing data. The configuration software structure described above makes it possible to do this by essentially reversing the configuration process. That is, with reference to Figure 13, the known configuration data 953 of a particular module is applied to the tables 955, 957 and 959 in order to read the functional parameters, operating parameters and interconnections for the module. The software then displays that module with the specified connections and characteristics. Once all of the configuration data for all of the modules is converted in this way, the programmed circuit is displayed on the computer monitor in one of the forms shown in Figures 16A or 16B, as desired.

If the configuration data being reviewed is found only in the configuration registers of an actual chip, then that data is first read out of the chip through the test module in a manner described above (see data path 722 of Figures 3 and 4). This is accomplished by use of the system of Figure 8, with the chip 922 containing the data being mounted on the evaluation board 920.

Additional illustrations, some in color, of computer monitor screens appearing during configuration of the chip described herein can be found in an article by Frank Goodenough, appearing in *Electronic Design*, October 14, 1994, beginning at page 63. The entirety of this article is incorporated herein by this reference.

Although the various aspects of the invention have been described with respect to its preferred embodiments, it will be understood that the invention is entitled to protection within the full scope of the appended claims.

IT IS CLAIMED:

1. A method of forming an analog circuit, comprising:

providing an integrated circuit chip having analog signal and configuration data connections, and a plurality of analog circuit modules which are individually configurable and interconnectable among a specified number of operational choices in response to control bits which are loaded through the configuration data connection and stored on the circuit chip,

displaying said circuit chip modules by individual symbols thereof spaced apart across a computer monitor screen,

in response to an operator selecting through the computer the use of one of said modules in the analog circuit being formed, displaying on the computer screen said operational choices for the selected module,

in response to the operator selecting through the computer certain ones of the displayed list of operational choices, generating appropriate ones of said control bits which carry out the selected operational choices on the circuit chip and displaying on the computer screen any resulting interconnections established between the selected module and any other of said plurality of modules,

repeating the foregoing two steps for others of the modules, one at a time, until all the desired of said operational choices have been made,

assembling the generated control bits into a form suitable for writing into said configuration register, and

writing the assembled bits into the configuration register of said integrated circuit chip through its configuration connection.

2. The method according to claim 1, additionally comprising, before writing the assembled bits into the configuration register, comparing in the computer the selected operational choices against a plurality of undesired combinations of choices, and, if any of said undesired combinations of choices are detected, displaying such on the computer monitor screen.

3. A method of forming an analog circuit, comprising the steps of:

providing an integrated circuit chip having signal input, signal output and configuration data connections and which includes:

an input module connected to a chip input connection, having an output line and at least one operational parameter that is configurable in response to a first group of control bits stored in a configuration register provided as part of the circuit chip,

a plurality of functional modules each having an input, an output, at least one analog function that is configurable in response to a second group of control bits of said register and at least one operational parameter for each such function that is configurable in response to a third group of control bits of said register,

an output module connected to an output connection, having an input line and at least

one operational parameter that is configurable in response to a fourth group of control bits,

a switching network for interconnecting the input module output line, the output module input line and the inputs and outputs of the functional modules, all in response to a fifth group of control bits, and

a configuration register into which said control bits may be loaded through the configuration connection,

displaying on a computer screen symbols of the input module, the output module and the functional modules without interconnections through the interconnecting switching network being shown,

in response to an operator designating a first one of said modules, generating appropriate ones of said control bits and displaying on the computer screen the configuration, operational parameter and interconnection choices for the designated module,

in response to the operator selecting among the configuration, operational parameter and interconnection choices, generating appropriate ones of said control bits and displaying on the computer screen wire interconnections between the designated module and other modules,

repeating the foregoing two steps for others of the modules until the desired circuit functions, interconnections and operating parameters are displayed on the computer screen,

assembling the generated control bits into a form suitable for writing into said configuration register, and

writing the assembled bits into the configuration register of said integrated circuit chip through the configuration connection.

4. A method of ascertaining an electronic circuit implemented by an integrated circuit chip having a plurality of analog circuit modules with individual functions and interconnections specified by configuration data stored on the circuit chip, comprising:

reading the configuration data from the circuit chip,

converting individual fields of that data into individual functions and interconnections of the analog circuit modules, and

graphically forming a schematic diagram of the electronic circuit implemented by the chip that shows symbols representing said individual functions and interconnections of the analog circuit modules.

5. The method of claim 4 wherein the converting of individual fields of data includes doing so by computer with a look-up table that relates potential functions and interconnections of the individual modules with unique fields of configuration data.

6. The method of claim 4, additionally comprising modifying the configuration data read from the circuit chip, updating the schematic diagram to conform to any functions or interconnections of the electronic circuit that are changed by the modification of the configuration data, and reloading the modified configuration data into the circuit chip.

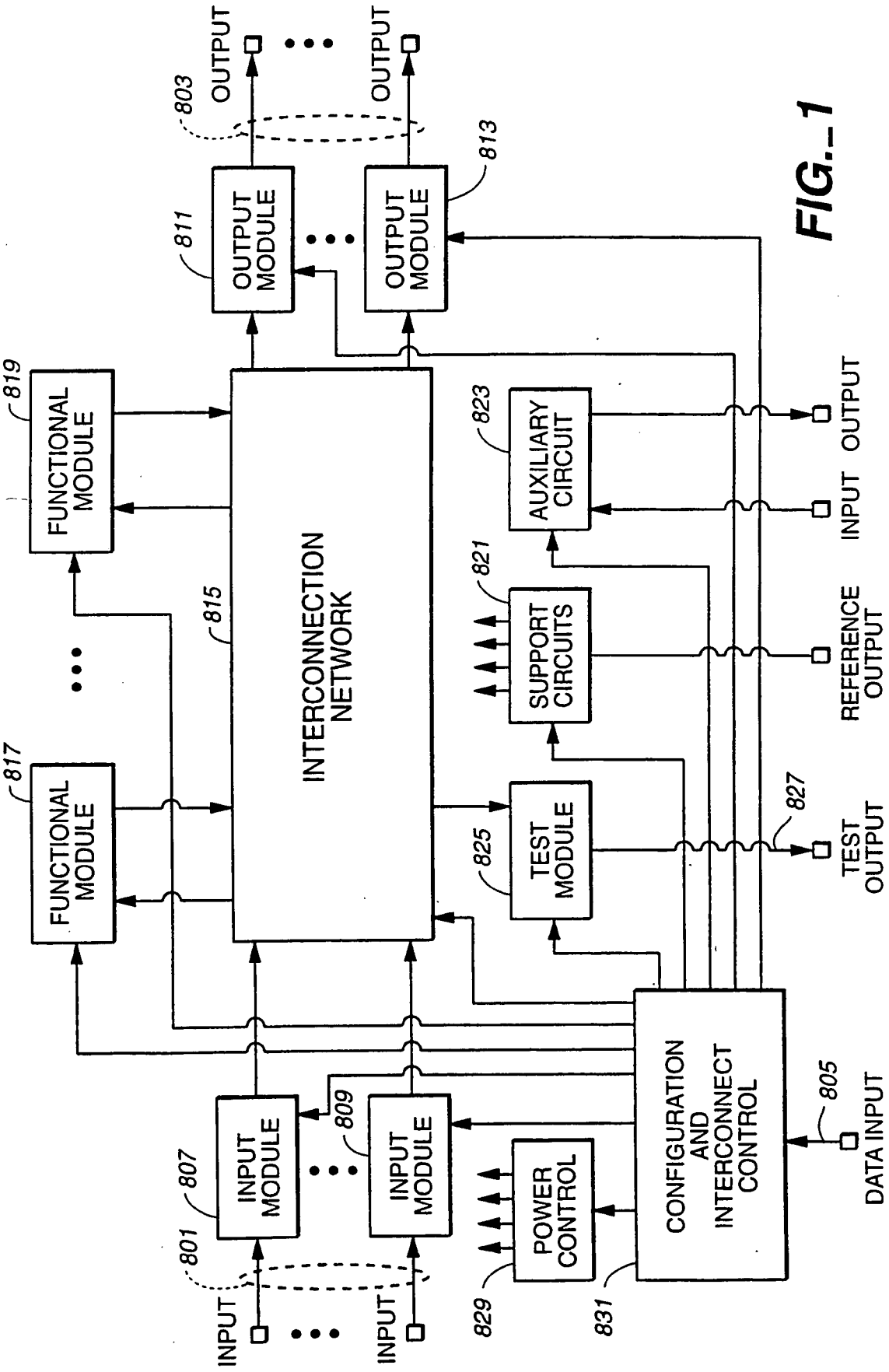

FIG._1

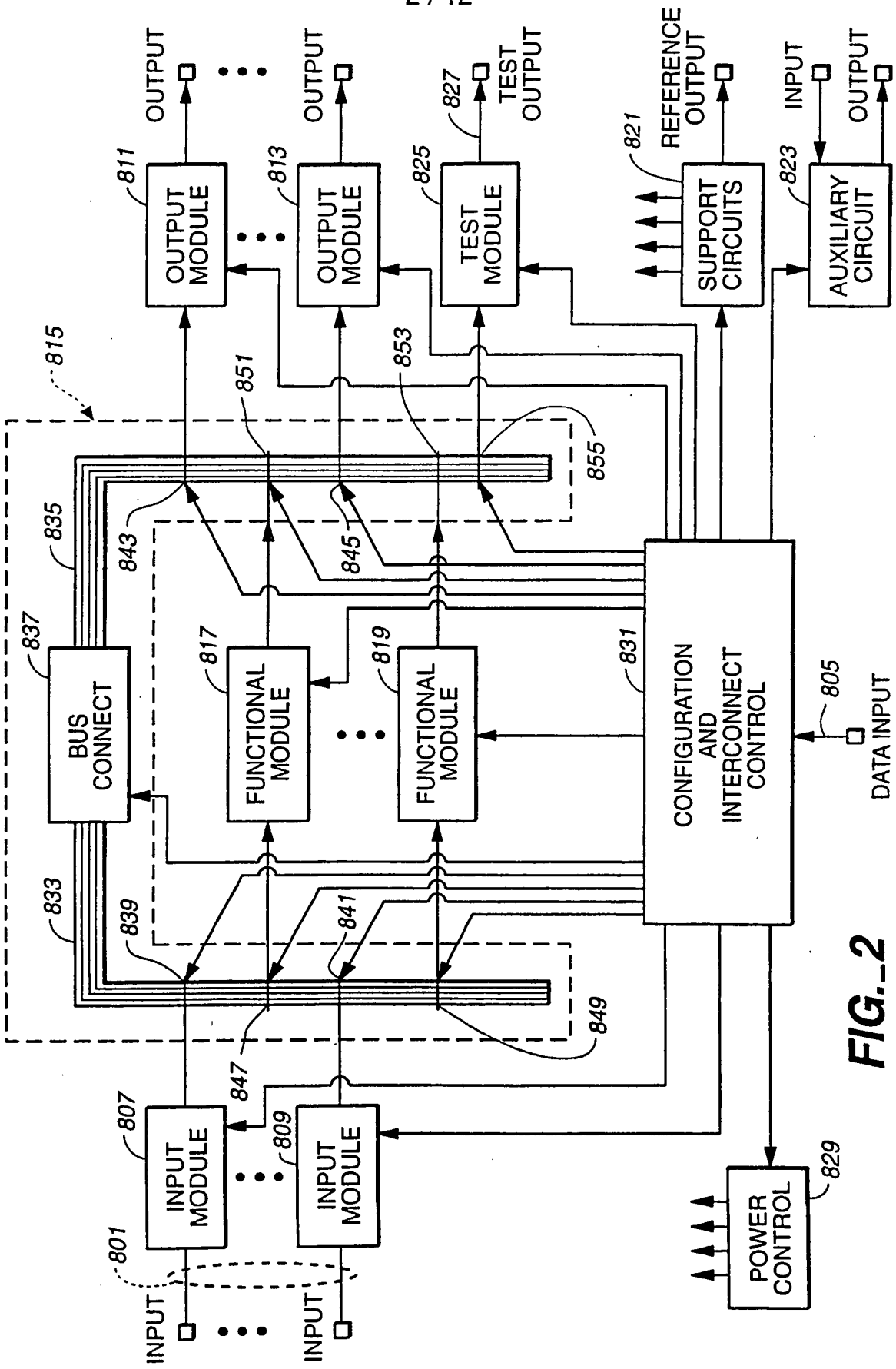

FIG._2

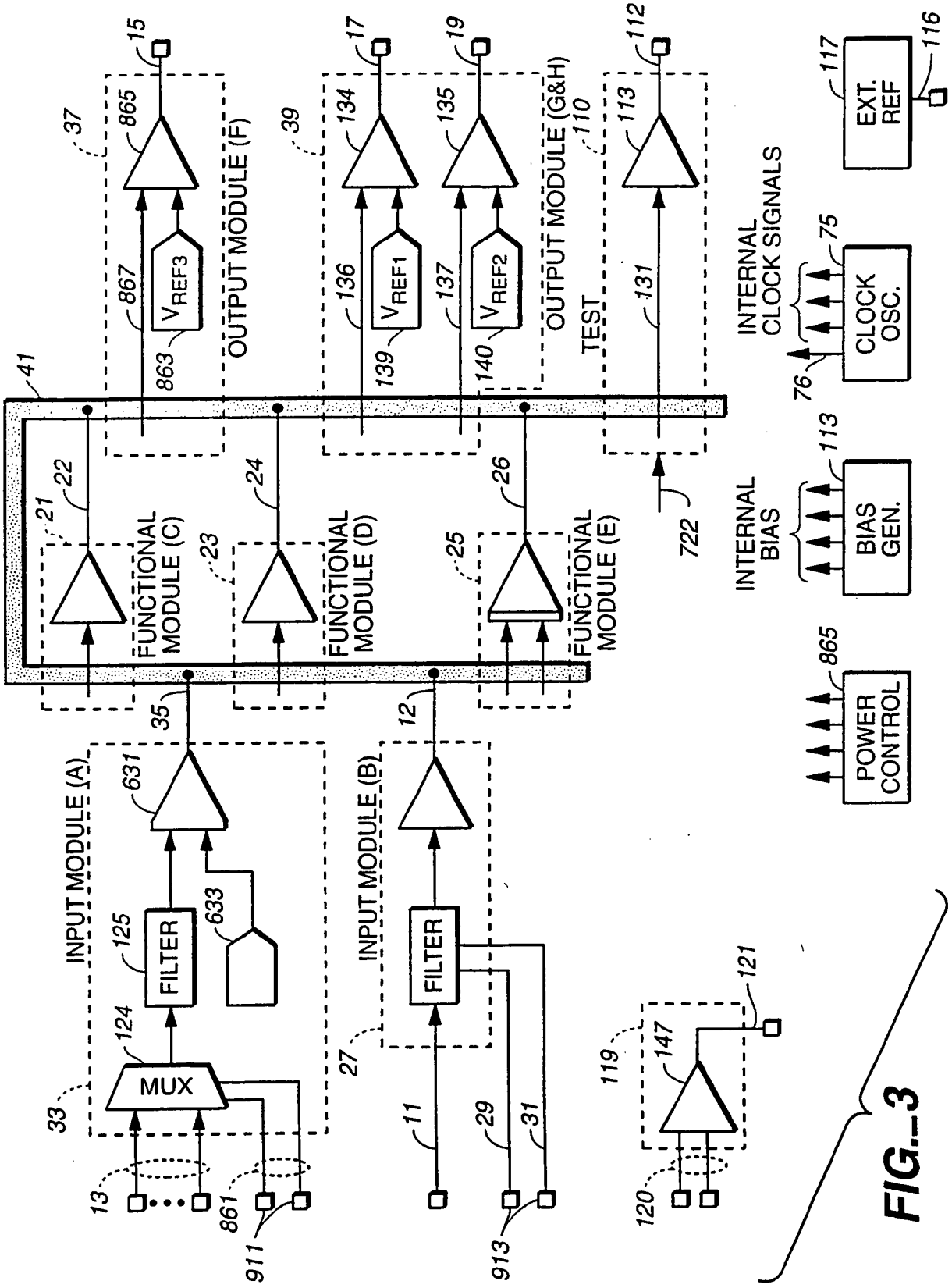

FIG._3

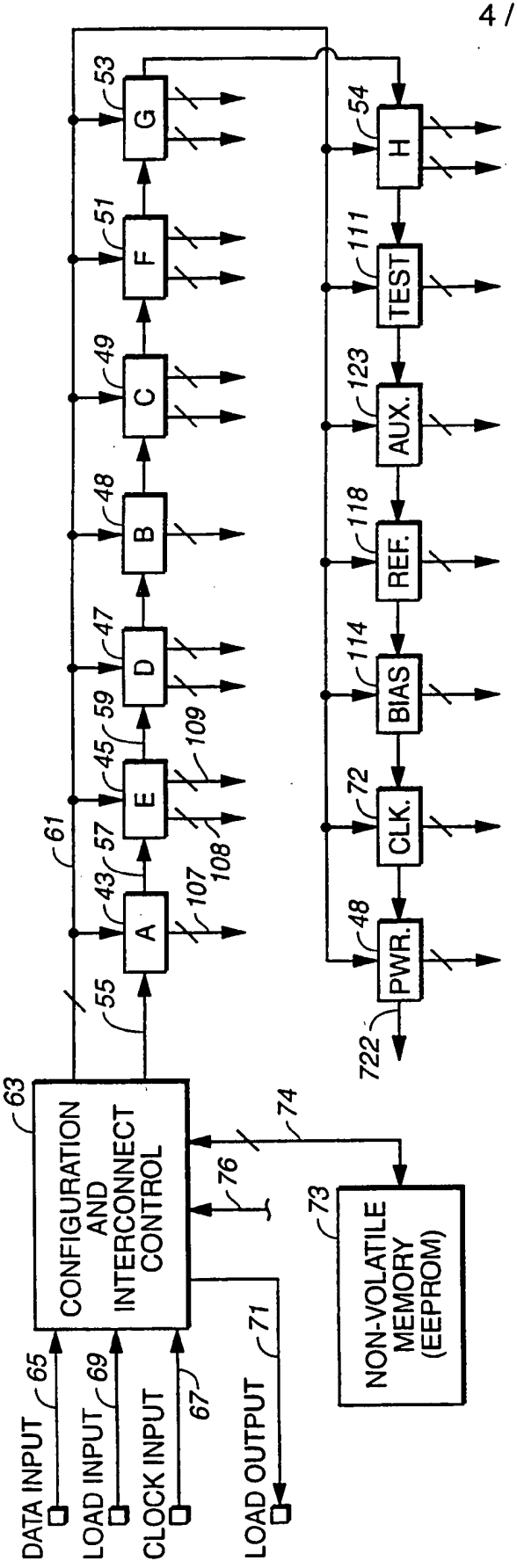

FIG._4

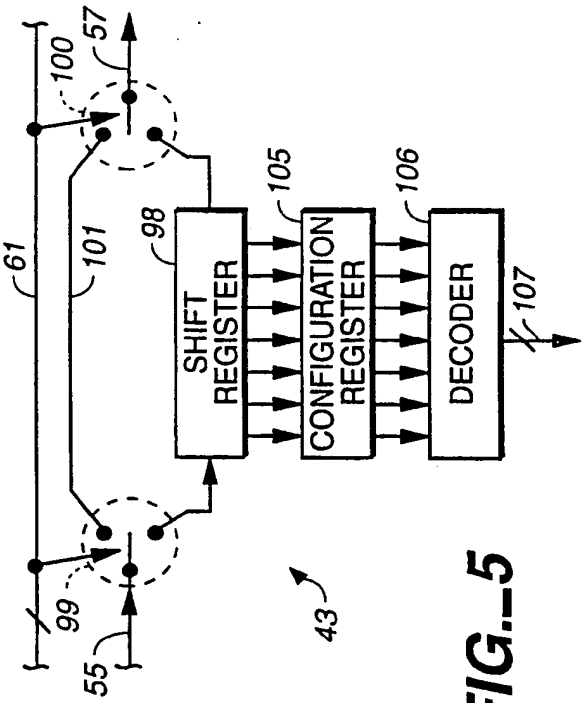

FIG._5

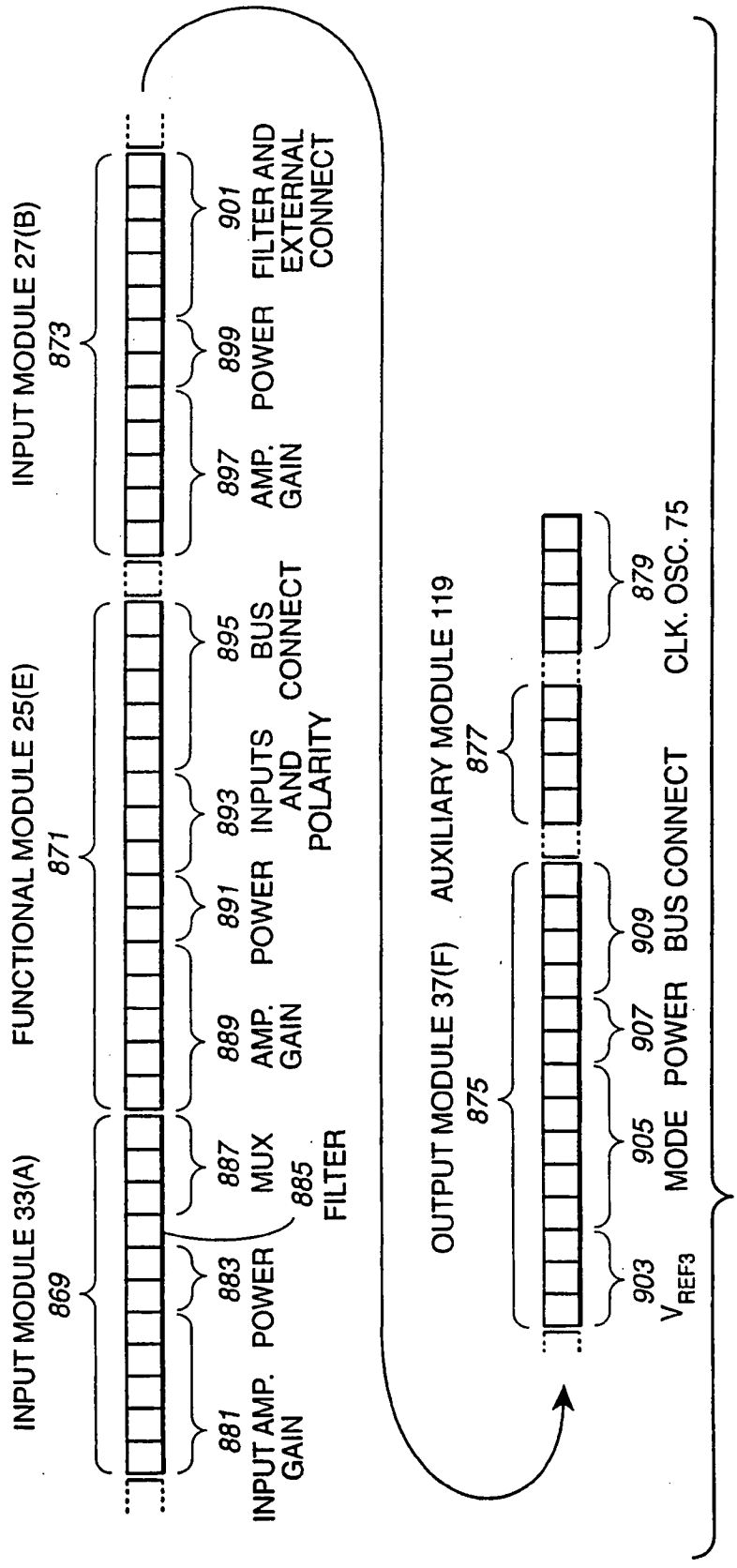

FIG._6

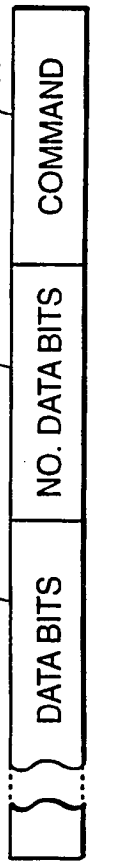

FIG._7

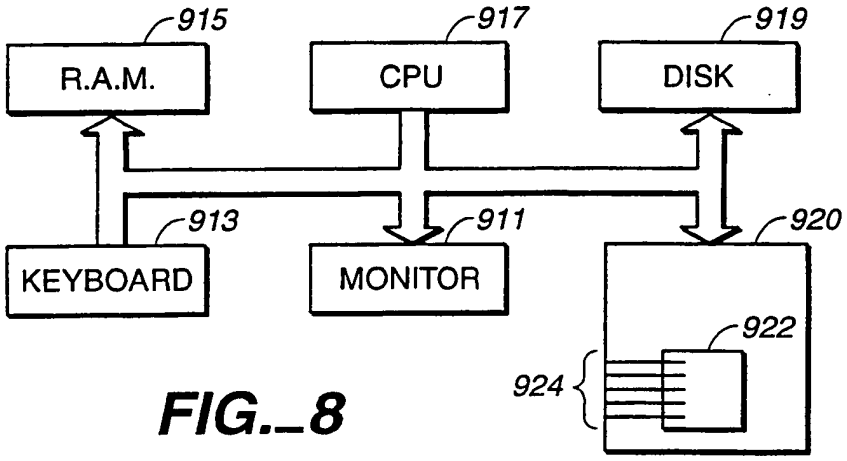

FIG._8

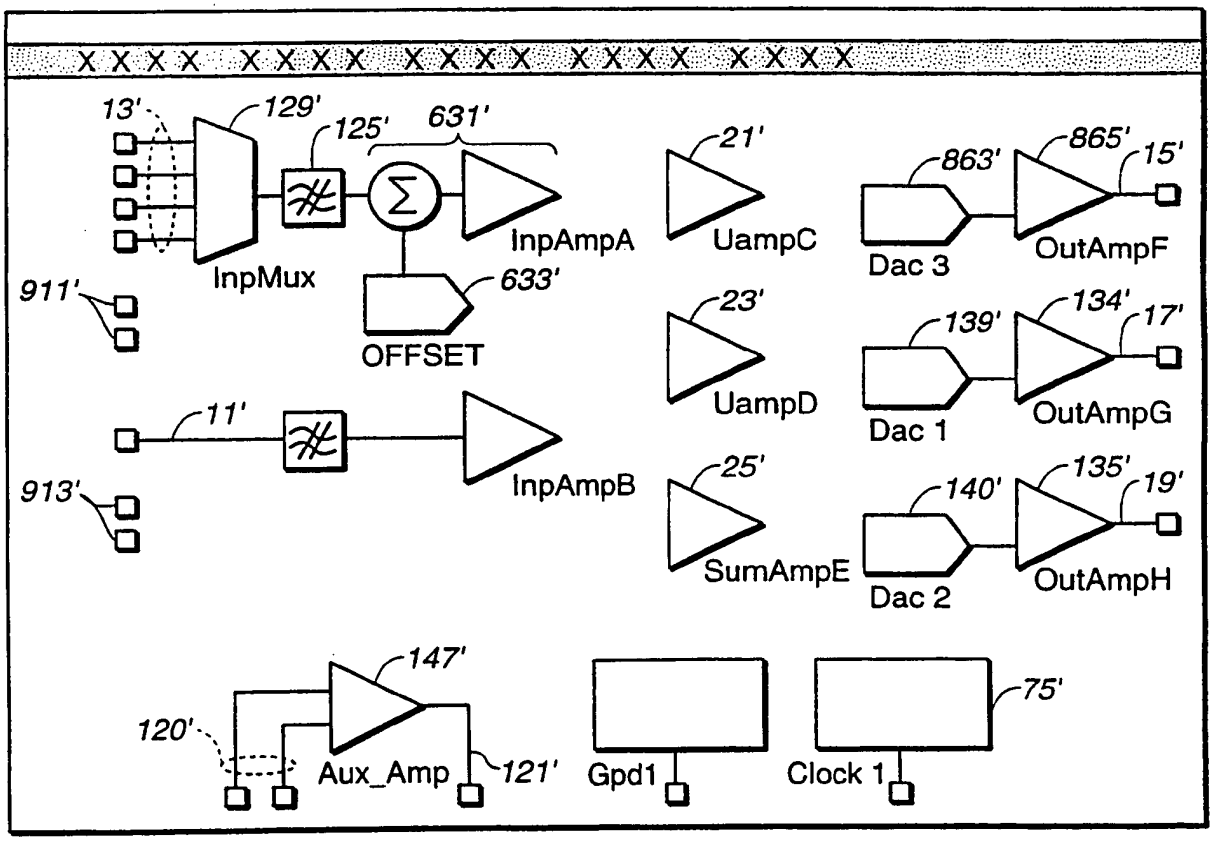

FIG._9

FIG._10A

FIG._10B

FIG._10

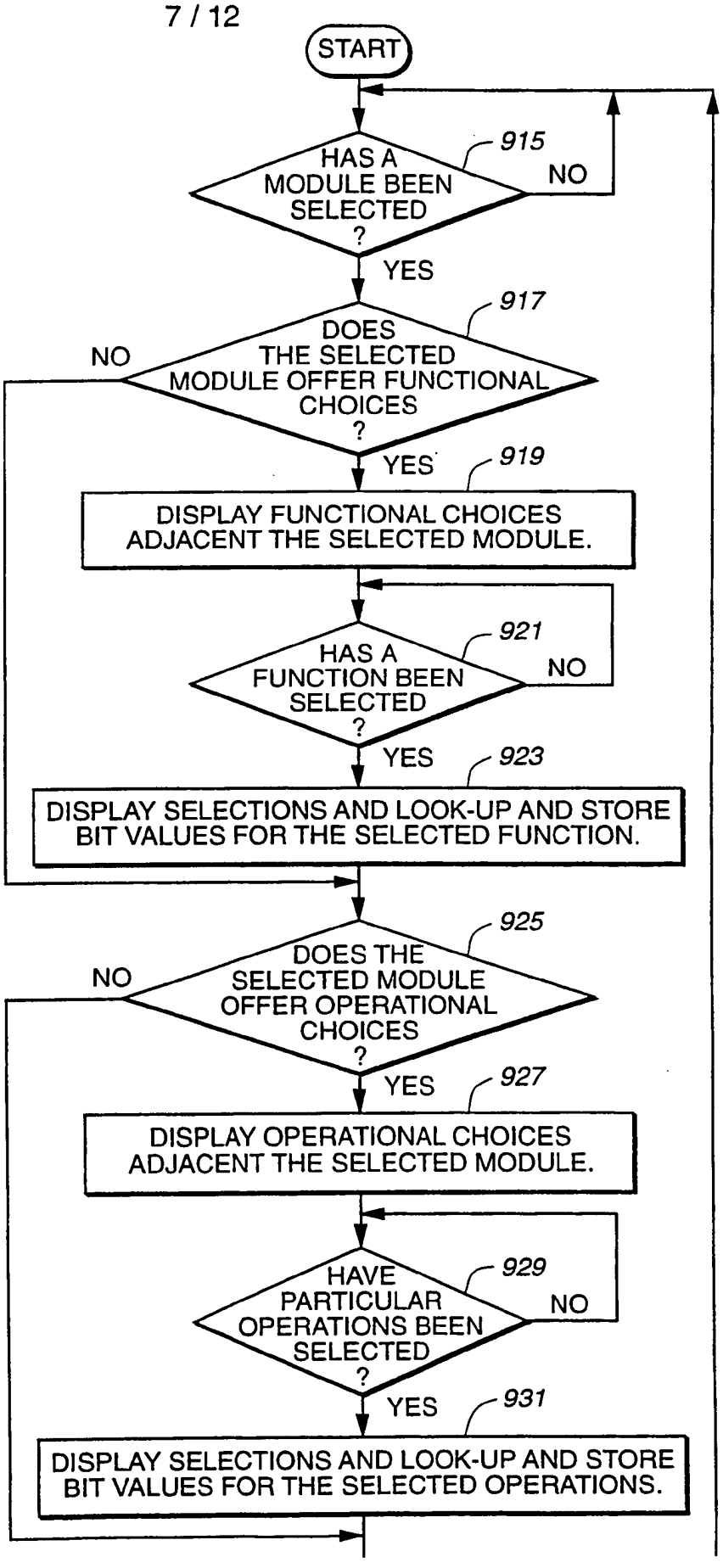

FIG._10A

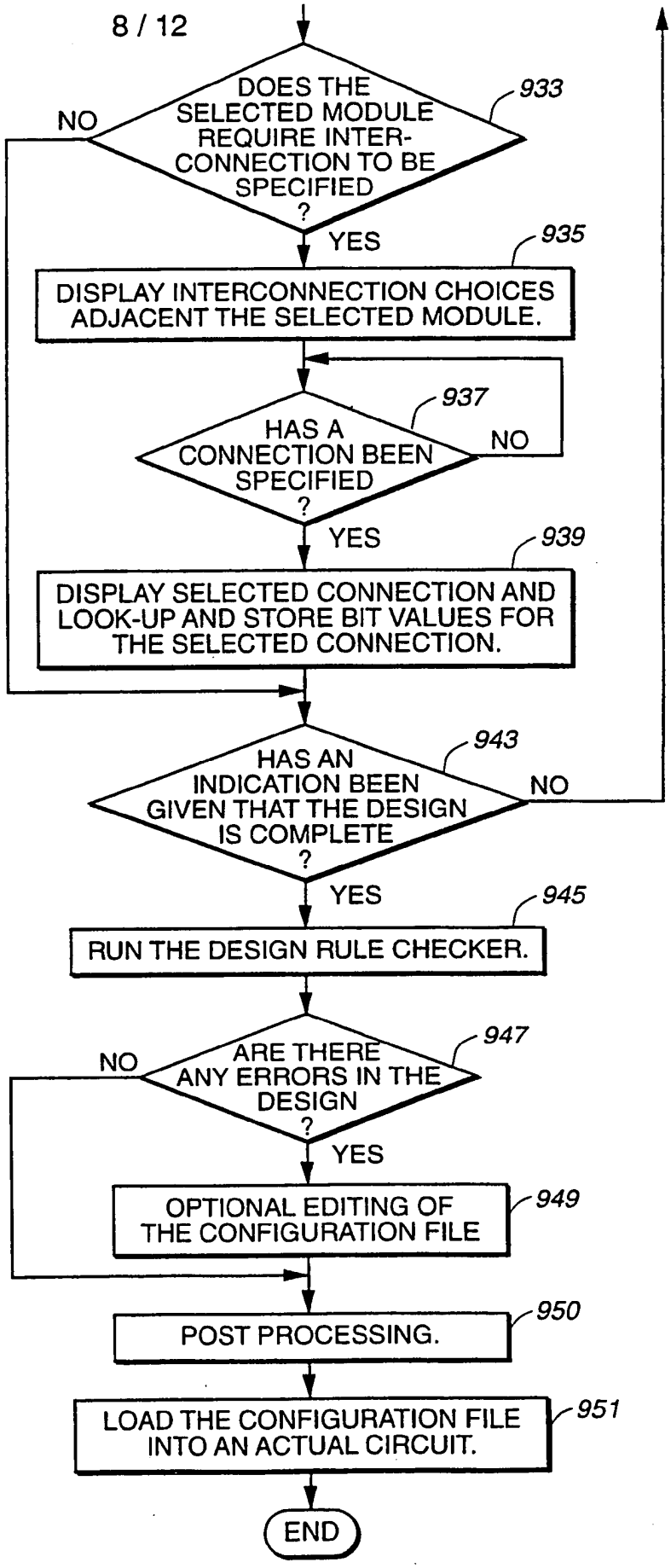
DOES THE SELECTED MODULE REQUIRE INTER-CONNECTION TO BE SPECIFIED ?
933
NO
YES
DISPLAY INTERCONNECTION CHOICES ADJACENT THE SELECTED MODULE.
935
HAS A CONNECTION BEEN SPECIFIED ?
937
NO
YES
DISPLAY SELECTED CONNECTION AND LOOK-UP AND STORE BIT VALUES FOR THE SELECTED CONNECTION.
939
HAS AN INDICATION BEEN GIVEN THAT THE DESIGN IS COMPLETE ?
943
NO
YES
RUN THE DESIGN RULE CHECKER.
945
ARE THERE ANY ERRORS IN THE DESIGN ?
947
NO
YES
OPTIONAL EDITING OF THE CONFIGURATION FILE
949
POST PROCESSING.
950
LOAD THE CONFIGURATION FILE INTO AN ACTUAL CIRCUIT.
951
END

FIG._10B

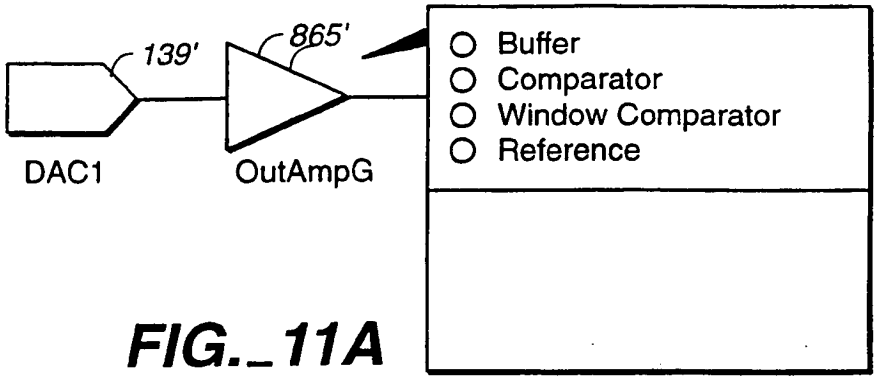

FIG._11A

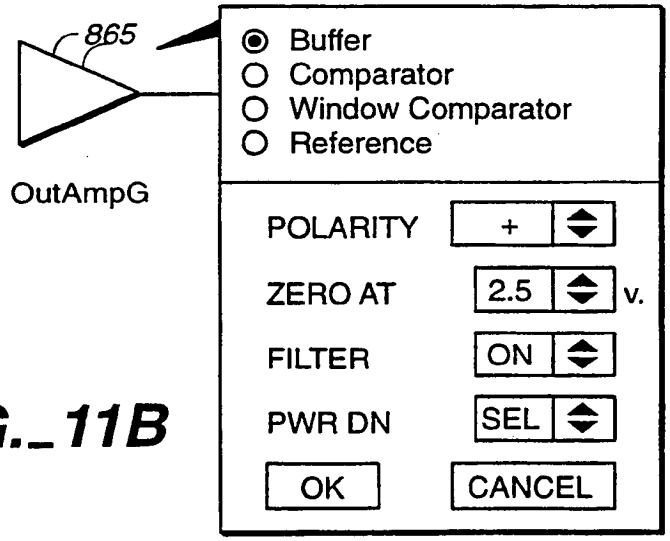

FIG._11B

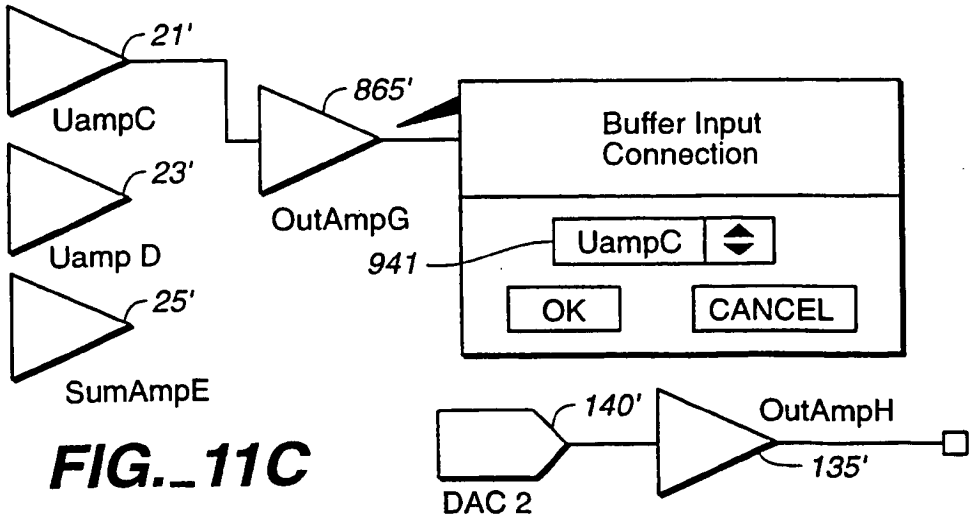

FIG._11C

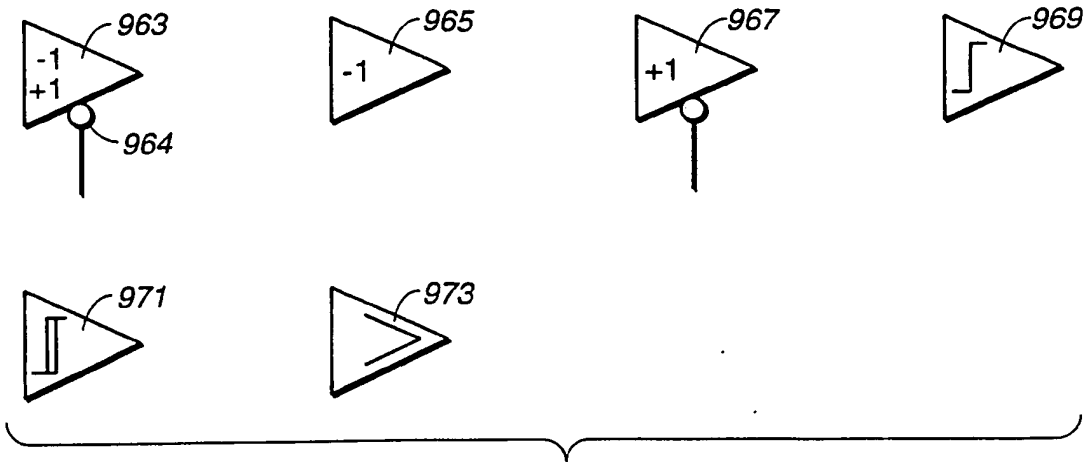

FIG._12

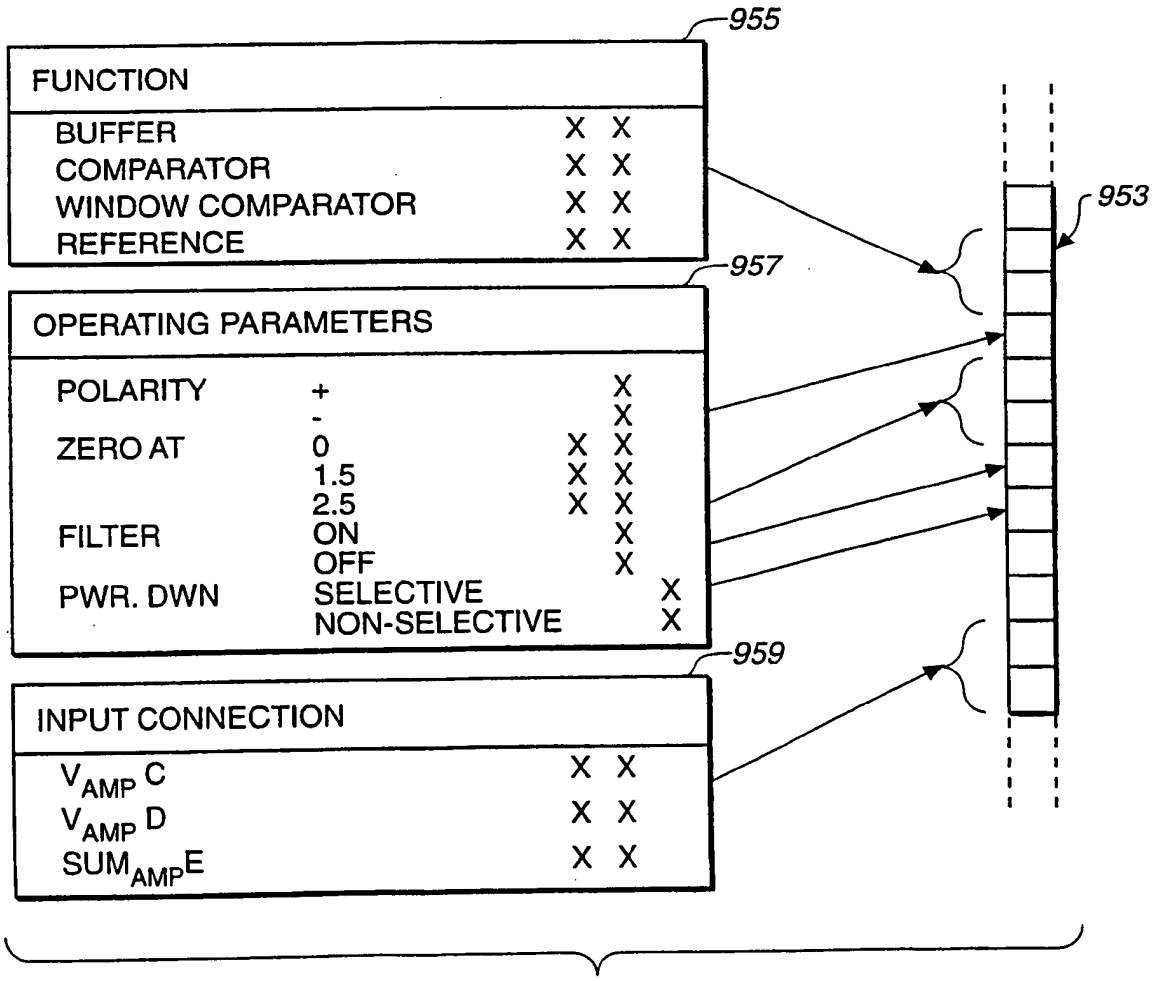

FIG._13

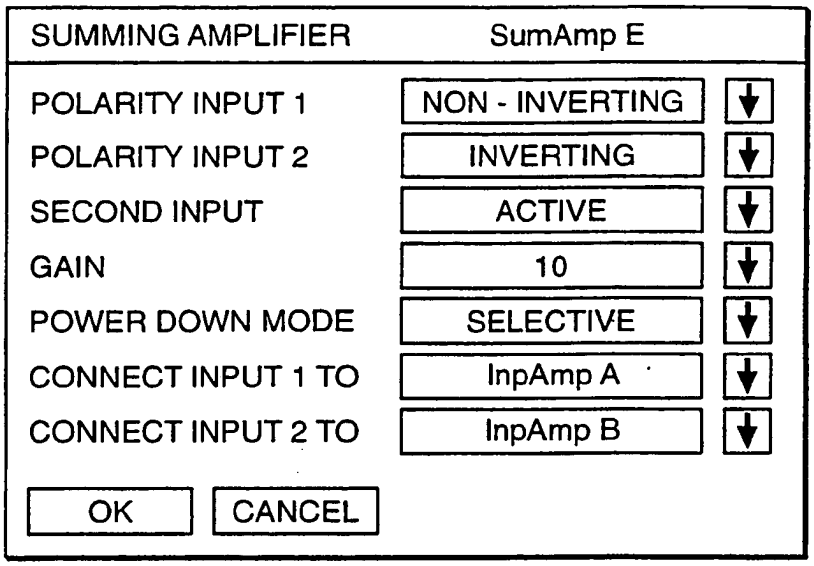

FIG._14

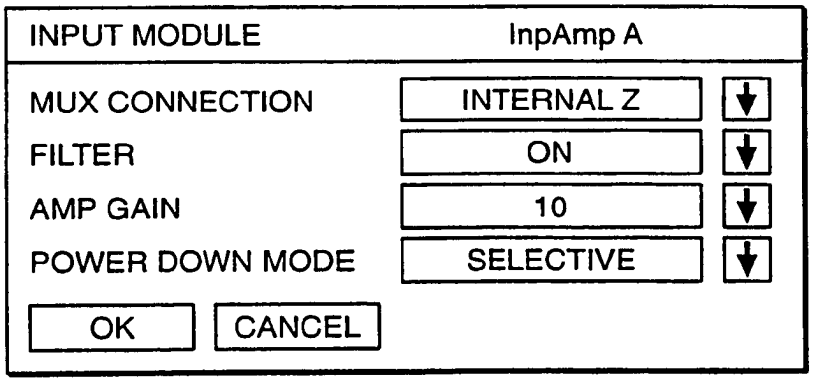

FIG._15

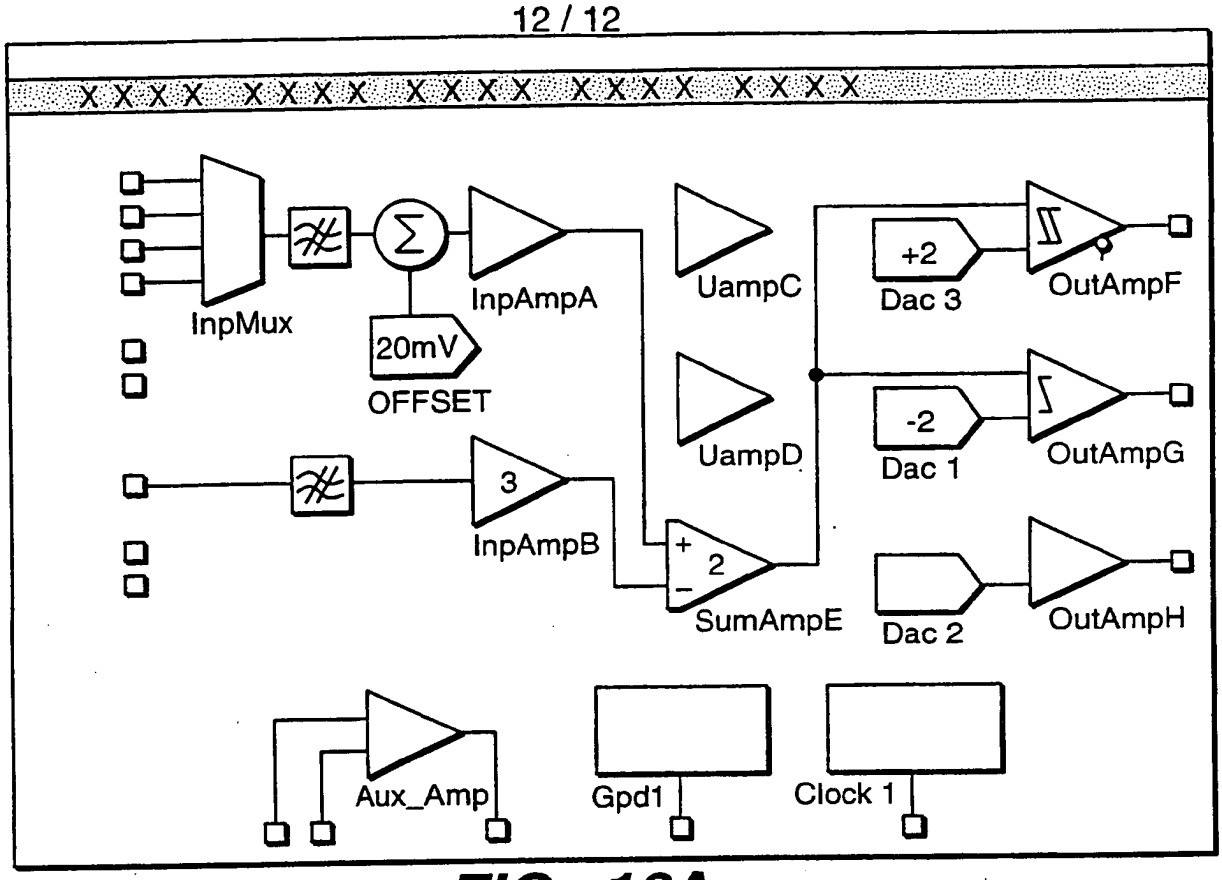

FIG._16A

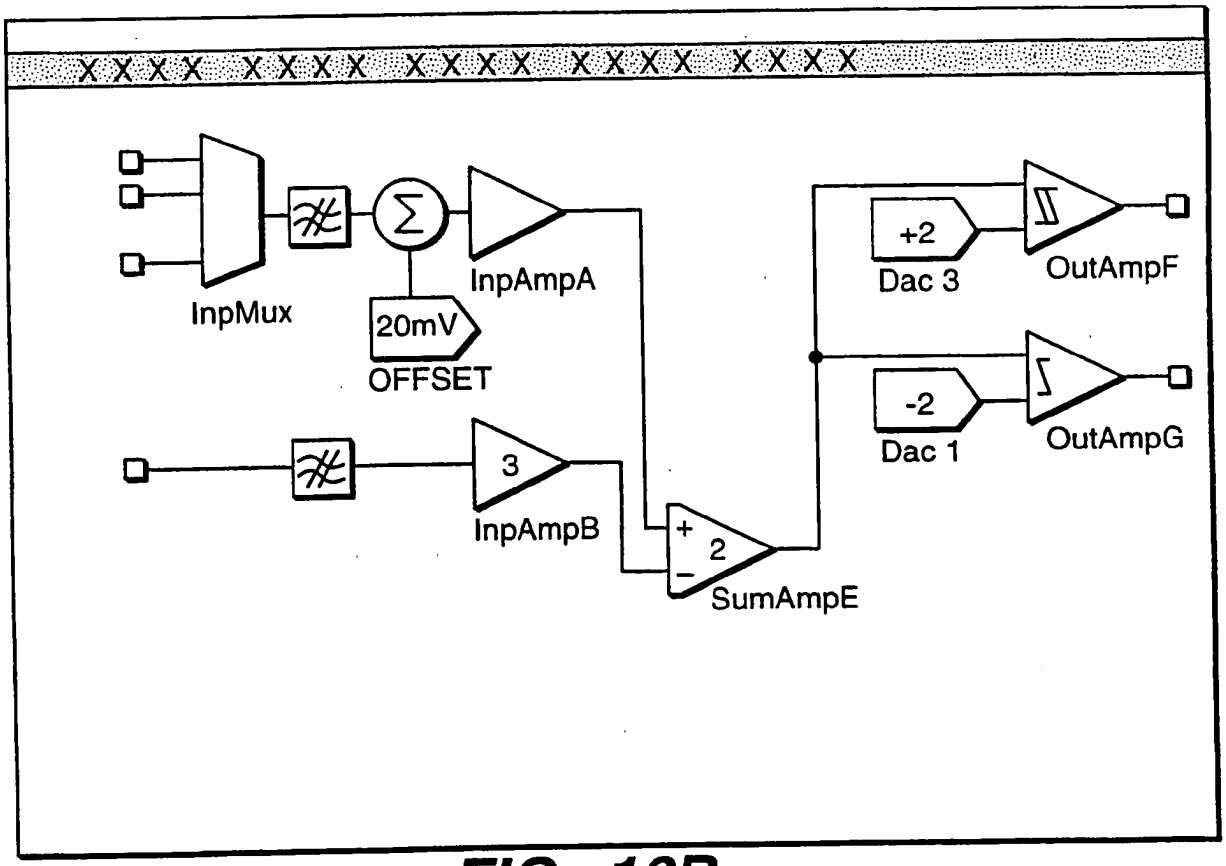

FIG._16B

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
WO-A-9009639	23-08-90	EP-A-	0411090	06-02-91
		GB-A,B	2229300	19-09-90
		JP-T-	3504651	09-10-91
		US-A-	5224055	29-06-93
EP-A-450863	09-10-91	AU-B-	639543	29-07-93
		AU-A-	7405191	10-10-91
		CN-A,B	1055436	16-10-91
		EP-A-	0450866	09-10-91
		GB-A,B	2242801	09-10-91
		GB-A,B	2246666	05-02-92
		JP-A-	5175466	13-07-93
		JP-A-	5145038	11-06-93
		US-A-	5196740	23-03-93

INTERNATIONAL SEARCH REPORT

Interna . .l Application No
PCT/US 95/06527

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F17/50 G06G7/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO,A,90 09639 (PLESSEY OVERSEAS LIMITED) 23 August 1990 see page 2, line 20 - page 3 see page 6, line 7 - line 26 see page 10, line 12 - page 16, line 19; figures 1,7-9 ---	1-6
Y	EP,A,0 450 863 (PILKINGTON-ELECTRONICS LIMITED) 9 October 1991 see column 1, line 31 - column 3 see column 6, line 35 - line 41; claims 1,5,6; figure 1 --- -/--	1-6

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 1995	27.09.95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Guingale, A

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	ELECTRONIC DESIGN , vol. 42, no. 21, 14 October 1994 CLEVELAND OH US, pages 63-73, GOODENOUGH 'analog counterparts of fpgas ease system design' cited in the application see the whole document -----	1-6

1